56F8006

Preliminary Chip Errata

56F8006 Digital Signal Controller

This document reports errata information on chip revision A. This document is a pre-publication draft.

Chip Revision A Errata Information:

The following errata items apply only to Revision A 56F8006 devices. These parts are marked with 1M53M.

Errata Number	Description	Impact and Workaround
1.	If the Computer Operating Properly (COP) is used to wake the device from the Partial Power Down (PPD) mode, the COP may count down too quickly.	Impact: The device may not wake from the PPD mode reliably. Workaround: 1.0 Use the RTC timer to wake from the PPD mode to the Run mode, rather than the Computer Operating Properly (COP) or use a timeout longer than 100MS for the COP to wake the device from Partial Power Down mode. 2.0 The COP may be used to bring the device out of PPD mode if the COP is driven by the low power oscillator rather than by a crystal.
2.	The internal relaxation oscillator does not meet the specifications for frequency.	Impact: Peripherals may operate with unexpected timing. Workaround: If stricter timing is required, use an external crystal, resonator, or oscillator module of the required frequency specification.
3.	The ADC Conversion Complete interrupt is asserted and then removed if sample_select ping-pongs to other ADC register-set prior to the CPU servicing the interrupt request.	Impact: The ADC interrupt signal may not interrupt the core. Workaround: Make the ADC a higher priority interrupt or poll the ADC in a timer or PWM interrupt handler rather than use the ADC interrupts.
4.	A hardware trigger generated through a PGA to an ADC may upset the use of Software triggers with the PGA.	Impact: Incorrect triggering of the ADC by the PGA may result in wrong data from the ADC. Workaround: Avoid the use of the software trigger mode of the PGA.

Chip Revision A Errata Information:

The following errata items apply only to Revision A 56F8006 devices. These parts are marked with 1M53M.

Errata Number	Description	Impact and Workaround
5.	When both PGAs are enabled and hardware triggers are used, if PDB both trigger A and trigger B are enabled with delay A very close to delay B, then the ADC conversion complete flag for the specified set of ADC status and control register/ data result register may not be set correctly.	Impact: With PGA hardware trigger mode enabled in both PGAs, each PDB trigger signal will cause each PGA to generate a pre-trigger signal to both ADCs. This results in the ADC pretrigger signal contention and the sample_select inside the ADCs to toggle and cause the wrong ADC status and control register to control the conversion. Workaround: Configure both ADC status and control registers in each ADC to the same value (that is, ADCSC1A=ADCSC1B) and then check the COCO flag bits in both ADC status and control registers for each ADC.

Errata Sheet History

Previously Documented in Past Errata Sheets	Correction
0	Initial release
1	Added workaround for Errata Number 1
2	Added Errata Number 5

THIS PAGE IS INTENTIONALLY BLANK

How to Reach Us:

Home Page:
www.freescale.com

Web Support:
http://www.freescale.com/support

USA/Europe or Locations Not Listed:
Freescale Semiconductor, Inc.
Technical Information Center, EL516
2100 East Elliot Road
Tempe, Arizona 85284
+1-800-521-6274 or +1-480-768-2130
www.freescale.com/support

Europe, Middle East, and Africa:
Freescale Halbleiter Deutschland GmbH
Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
www.freescale.com/support

Japan:
Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku,
Tokyo 153-0064
Japan
0120 191014 or +81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:
Freescale Semiconductor Hong Kong Ltd.
Technical Information Center
2 Dai King Street
Tai Po Industrial Estate
Tai Po, N.T., Hong Kong
+800 2666 8080
support.asia@freescale.com

For Literature Requests Only:
Freescale Semiconductor Literature Distribution Center
P.O. Box 5405
Denver, Colorado 80217
1-800-441-2447 or 303-675-2140
Fax: 303-675-2150
LDCForFreescaleSemiconductor@hibbertgroup.com

MC56F8006E
Rev. 2
04/2010